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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,583	02/05/2004	Douglas A. Larson	501296.01 (30266/US)	6732

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,583	LARSON ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6/19/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-43 have been presented for examination in this application. In response to the last office action, claims 1-3,11-13,21-23,32,36,40 have been amended, claims 5-10,16-20,26-31 have been canceled. As the result, claims 1-4,11-15,21-25,32-43 are pending in this application.

Claims 1-4,11-15,21-25,32-43 are rejected.

All rejections and objections not explicitly repeated below are withdrawn.

Applicant's amendments/remarks filed 9/19/06 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

The information disclosure statements filed 9/19/06 fails to comply with the provisions of 37 CFR 1.97, 1.98 because it does not list any prior art to be considered. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,4,11,14-15,21,24-25,32-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), and further in view of Zumkehr (US 6901494).

As in claim 1, Zimmerman describes a memory hub for a hub-based memory module (Zimmerman's Fig 2: MMB, paragraph 17), comprising: first and second link interfaces for coupling to respective data busses; a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces (Zimmerman's Fig 2, links 112 on both sides of MMB; paragraphs 15);

Zimmerman does not disclose the claim's aspect of a bidirectional data bus operable to transfer both read and write data. However, Goodwin discloses a mechanism in which multiple memory devices are connected to a bidirectional bus as depicts in Goodwin's Fig 2: Expansion devices. It would have been obvious to one of ordinary skill in the art at the time of invention to include bi directional bus mechanism as suggested by Goodwin in Zimmerman's system thereby further allow read and write data in expansion devices such as memory devices to be transferred effectively over the same bidirectional data bus (Goodwin's column 1 lines 10-35). Zimmerman

discloses first and second link interfaces for coupling to respective portions of the bus the portion of the data bus (i.e Host side and downstream sides of the links 132, 142, each segment represent a portion of the data bus). Goodwin further discloses the expansion memory #216 having the direct data path (SCL 236 through which data is transferred between the first (i.e link to expansion memory 215) and second link (i.e link to expansion memory 218) interfaces, Zimmerman and Goodwin do not expressly disclose the claim's detail of bypath data path. However, Zumkehr's discloses a bypath data path having a write bypass circuit coupled to the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path (Zumkehr's Fig 7 #730 discloses the circuits in the translator hub providing a direct data path, in which the write data received by the translator hub (Fig 2: #220) is immediately and directly forwarding to the downstream device; Zumkehr's Fig 6 discloses a multiplexer (i.e write by pass circuit) that allowing temporary stored the write data while allowing the read data to be transferred through the direct data path, directly to the upstream device; subsequently the multiplexer recouple the stored write data and sending to the downstream device; Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller hub circuits and methods as suggested by Zumkehr in Zimmerman's system to allow transferring read data while

temporary storing write data, thereby resulting in more efficiently usage of the memory bus in the system (Zumkehr's column 6 lines 35-60; read and write data transferring through the same bidirectional data bus Fig 3: #350 data signals).

As in claim 4, Zimmerman's Fig 5 describes a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

Claims 11,21,32,36 rejected based on the same rationale as in the rejection of claim 1.

Claims 14,24 rejected based on the same rationale as in the rejection of claim 4.

As in claim 15, Zimmerman discloses a memory controller (Fig 2: MMB) coupled to a data path through a memory controller bus (Zimmerman's Fig 2: 112); and further coupled to at least one of the plurality of memory devices through a memory device bus (MMB couples to memory device DRAM obviously vie DRAM memory device bus), a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device (Zimmerman's paragraph 15 discloses the buffered memory modules/controller logic to store the memory requests and to store the memory data receiving from the host).

Claim 21 rejected based on the same rationale as in the rejection of claim 1.Zimmerman's Fig 1 further discloses a processor (Zimmerman's Fig 1: #20) and processor bus connecting the processor to the system controller (Zimmerman's Fig 1: #30 MCH), which obviously having associating ports connecting to peripheral devices such as memory data storage devices

(Zimmerman's Fig 2: DRAM); a memory module (Zimmerman's Fig 3a) comprising memory hub (Fig 2: MMB). The remaining limitation of claim 21 is rejected based on the same rationale as of claim 1.

Claim 25 rejected based on the same rationale as of claim 15.

As in claim 33, Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be issued earlier and, to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals.

As in claim 34, Zumkehr describes translator circuit to translate a write command to an sdram write command for the memory device, in addition to the FIFO queue for other write commands being received (Zumkehr's column 5 lines 5-12).

As in claim 35, Zimmerman discloses wherein the memory system includes a plurality of memory modules coupled in series on the memory bus (Zimmerman's Fig 2 DRAM memory modules #120, #130 in serial on the memory bus), and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed (Zimmrman's Fig 2 discloses writing to memory module #130 located downstream from memory module #120 in which the read data is accessed by the host #110).

Claim 37 rejected based on the same rationale of claim 33.

As in claim 38, Zumkehr's describes the write buffer to temporary store write data request (zumkerhr's Fig 3: #330).

As in claim 39, the claim recites wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus. Zumkehr further describes the write buffer in MMB is provided to temporary store data from host and thus decoupling the host to handle another accessing data on the memory bus (Zumkehr's Fig 5)

Claim 40 rejected based on the same rationale as of claim 1. Zimmerman further discloses a memory system with multiple buffered memory modules; each memory buffer module can buffer write and read command issued from the host (Fig 2: #110). Thus the host can continue issuing commands to these buffered memory modules in concurrently manner, that is the read command can be issued to memory module Fig 2: #130 before issuing the write command to memory module Fig 2: #120.

As in claim 41, the claim rejected based on the same rationale as of claim 40. Zumkehr's column 7 lines 17-23 further discloses the write command received by the translator circuit must be delayed for a time period and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals. Therefore the collision on the bi-direction data bus can be averted.

As in claims 42-43, Zumkehr discloses the write data is stored temporary in Fig 3: #330 to avoid the collision with the read data receiving from bi-directional data signal Fig 2: 350's

data signals (claim 42); wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus (claim 43; Zumkehr discloses a FIFO to temporary store write commands (i.e sending the write data of the first write command to at least one memory module, receiving read command, storing the data of the second write command in the FIFO before decoupling and allowing the data of a read travels through the memory bus (from Fig 3: #350 data signals to the host, Fig 3: #310 data signal).

Claims 2-3,12-13,22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), Zumkehr (US 6901494) as applied to claims 1,11,21 respectively, and in view of Garcia et al (US 6782435).

As in claim 2, although Zumkehr's Fig 6: #650 discloses the multiplexer providing the directly data path (read data) and the bypass data path (write data), Zumkehr does not expressly disclose the claim's detail of the multiplexer. However, Garcia's Fig 2 teaches in detail a multiplex circuit comprises a multiplexer, a bypass selection signal, and a register to temporary store write data being received. It would have been obvious to one of ordinary skill in the art at the time of invention to include the temporary storage and the multiplexer circuits as suggested by Garcia in Zimmerman's system to temporary reordering the transmitting data thereby allowing accessing memory device with minimum latency and maximizing the throughput of he overall system (Garcia's column 1, lines 48-62).

As in claims 3, the claim recite wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register. The claim rejected based on the same rationale as in the rejection of claim 2.

Claims 12,22 rejected based on the same rationale as of claim 2.

Claims 13,23 rejected based on the same rationale as of claim 3.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

Regarding remarks on pages 11-12 for the Zimmerman's expressly teaching of the bidirectional data bus. It's mooted in view of the new reference Goodwin et al, new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Regarding the remark on pages 12-17, Applicant contends that Zumkehr does not provide a direct data path for the write data to be provided to the down stream device (i.e the sdram device). Examiner respectfully disagrees. Zumkehr's Fig 6 discloses a multiplexer in the translator hub that provides a data path directly to the downstream device, when it received the write data sent from the host's Fig 3: #210; receiving at its buffer Zumker's Fig 3: #330 and sending directly to down stream devices Fig 3: #161. Examiner notes that the same mechanism is

disclosed in specification's Fig 3, that is host's data is received at a receiving buffer Fig 3: 302 and subsequently it is sent directly to down stream device.

Applicant contends that Zumkehr's buffering circuits do not provide avoiding the data collision between data heading the opposite directions on the bidirectional data paths. Examiner respectfully disagrees, Zumkehr discloses write buffers that temporary store write data of write requests so that the read data of the read command can be sent on the opposite direction toward the host on the same bidirectional bus, Fig 3: #350 data signals. Thus the write data toward the down stream device is temporary stored, delay and avoids the collision with the read data traveling in opposite direction on the same bidirectional data bus (see Zumkehr's column 6 lines 22-30).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
11/29/06